Development of a High-Rate, High-Resolution Detector for EXAFS Experiments

G. De Geronimo, P. O'Connor, R. H. Beuttenmuller, Z. Li, A. J. Kuczewski, D. P. Siddons

***Abstract*-- A new detector for EXAFS experiments is being developed. It is based on a multi-element Si sensor and dedicated readout ASICs. The sensor is composed of 384 pixels, each having 1mm^2 area, arranged in four quadrants of 12 x 8 elements, and wire-bonded to 32-channel front-end ASICs. Each channel implements low noise preamplification with self-adaptive continuous reset, high order shaper, band-gap referenced baseline stabilizer, one threshold comparator and two DAC adjustable window comparators, each followed by a 24-bit counter. Fabricated in 0.35µm CMOS dissipates about 8mW per channel. First measurements show at room temperature a resolution of 14 rms electrons without the detector and of 40 rms electrons (340eV) with the detector connected and biased. Cooling at -35C a FWHM of 205eV (167eV from electronics) was measured at the Mn-Kα line. A resolution of about 300eV was measured for rates approaching 100kcps/cm^2 per channel, corresponding to an overall rate in excess of 10MHz/cm^2. A channel-to-channel threshold dispersion after DACs adjustment of 2.5 rms electrons was also measured.**

I. Introduction

EXTENDED X-ray Absorption Fine Structure (EXAFS) experiments impose stringent requirements on a detection system, due to the need for processing ionizing events at a high rate, typically above of 10Mcps/cm^2, and with a high resolution, typically better than 300eV (35 rms electrons in Si).

The detection system here presented is being developed targeting these stringent requirements. It results from a cooperation, started in mid 2001, between the Instrumentation Division and the National Synchrotron Light Source (NSLS) of Brookhaven National Laboratory (BNL) and it will be used at one of the NSLS beam-lines. It is composed of a pixellated Si sensor fabricated at BNL and dedicated low-noise ASICs. The combination of high rate, high resolution and moderate complexity makes this system attractive in comparison to others [1,2]. In Sections II, III and IV the sensor, the interconnects and the electronics are described respectively. Section V reports on the first experimental results on single-quadrant prototypes.

Manuscript received November 11, 2002. This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC0298CH10886.

G. De Geronimo, P. O'Connor, R. H. Beuttenmuller and Z. Li are with the Instrumentation Division, Brookhaven National Laboratory, Upton, NY 11973 USA (telephone: 631-344-5336, e-mail: degeronimo@bnl.gov).

A. J. Kuczewski and D. P. Siddons are with the National Synchrotron Light Source, Brookhaven National Laboratory, Upton, NY 11973 USA (telephone: 631-344-2738, e-mail: siddons@bnl.gov).

II. Multi-Element Si Sensor

The Si sensor is composed of 384 pixels each having a 1mm × 1mm area, ideally arranged in four quadrants of 12×8 elements (Figure 1) and it was fabricated at the Semiconductor Detector Laboratory of the Instrumentation Division at BNL. The pixels were formed using p^+ boron implant (≈ 10^{14}/cm^2 at 40keV) on high resistivity (4-6kΩcm) n-type 250µm thick wafer with (111) orientation, with a planar n^+ ohmic contact on the back side using phosphorous implant (≈ 10^{14}/cm^2 at 150keV). A 100µm × 100µm aluminum bond pad was deposited in correspondence of each pixel, and the pattern of pads was developed to minimize the complexity of the wire-bonding operation (see Section III and Figure 4).

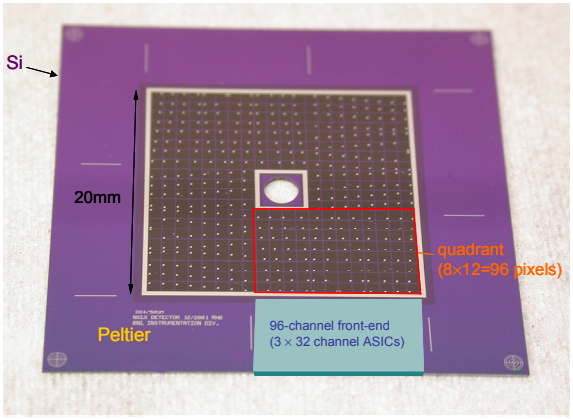

Fig. 1. Photo of the Si sensor (384 square pixels, 1mm² each). The ASICs sit on Si, off the long side of each quadrant; the Peltier elements sit on Si, on the remaining passive area. The center is opened for beam-through operation.

The silicon extends about 8mm on each side off the active area in order to accommodate the readout ASICs and the Peltier cooling elements.

The opening in the center allows beam-through measurements, where the beam hits the sample by flowing through the opening from the pixellated side, and the fluorescence from the sample is measured on the non-pixellated side. With this approach it is possible to place the sensor very close to the sample, thus increasing the solid angle and rate, with consequent reduction of the EXAFS measurement time.

In order to address the problem of pixel-to-pixel charge sharing and inter-pixel charge trapping [3], versions characterized by different pixel spacing of 10µm, 20µm, and 50µm were

built. A test structure with gaps variable from 6µm to 16µm was also fabricated end tested in order to evaluate how possible spectral degradations are related to the pixel gap. Two 8mm strip versions with 125µm pitch and gap of 10µm and 50µm, compatible with the ASICs, were also fabricated to expand the range of applications.

III. Mixed-Signal Front-End ASIC

A mixed-signal Application Specific Integrated Circuit (ASIC) targeted to this application was designed at the Instrumentation Division and fabricated in 0.35μm CMOS, dual-poly, four-metal (DP-4M) 3.3V technology. It is composed of 32 channels plus bias circuitry and digital interface, a total of 180,000 MOSFETs, and it dissipates about 8mW per channel. The layout, optimized for minimization of switching noise, measures 6.3×3.6mm^2 (Figure 2).

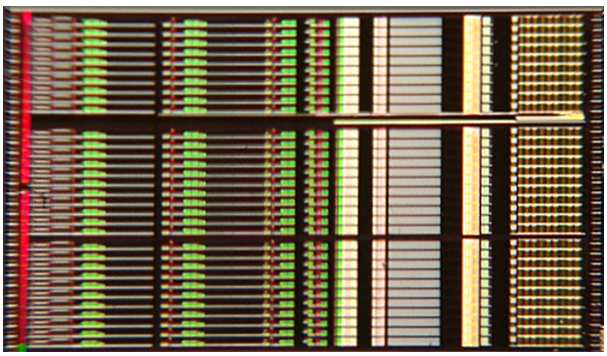

Fig. 2. Photo of the 32 channel ASIC, composed of 180,000 MOSFET. Three ASICs serve one quadrant (96 pixels) of the Si sensor.

Each channel implements (Figure 3) a low-noise preamplifier, a high order shaper with baseline stabilizer, one threshold and two window discriminators with DACs for fine adjustment, one counter per discriminator. A detailed description of the electronics is reported below.

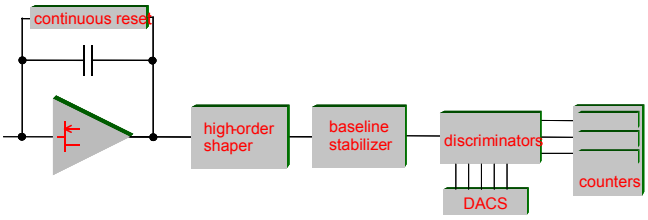

Fig. 3. Simplified schematic of one channel of the ASIC.

The preamplifier has a p-channel input MOSFET with W/L=400/0.35, I_d=850µA, V_{ds}=800mV, g_m=8.6mS and C_g=620fF. The p-channel was selected because of its lower 1/f noise when compared to the n-channel, and the size was optimized taking into account its operating regime. The input parasitic capacitance (pad plus wire-bond) ranges around 270fF to 420fF, depending on the wire-bond length (see Section IV).

The preamplifier implements a n-channel MOSFET in feedback operating in saturation to realize a low-noise fully compensated continuous reset circuit of the type described in [4]. The configuration is self-adaptive to leakage currents from the sub-pA to the nA, and contributes at most (when operated in weak inversion) a noise comparable to the one from the leakage current of the pixel. It provides a charge gain of 32. A cascade of two of these stages, the second based on p-channel MOSFET in feedback provides an overall gain of 32×32=1024 from the detector to the input of the first stage of the shaper. The 192kΩ feedback resistor of the following shaper thus contributes with an equivalent input shot noise of 240fA.

The second and third stage of the shaper provide two pairs of complex conjugate poles, realizing a 5th order complex semigaussian shaper. The high order shaper was chosen for its better noise filtering performance (up to 2.6 times compared to a low order) in a regime where the peaking time is set by the rate and the white series noise of the input MOSFET is the dominant component [5]. The output stage adds a gain of 4 and its output baseline is referenced to a bandgap circuit and fed back to the input of the second stage of the shaper through a slew-rate limited follower and a very low frequency filter, thus realizing a BLH configuration [6] for the baseline stabilization. The analog processing chain has settable peaking time (0.5µs, 1µs, 2µs, 4µs) and settable gain (750mV/fC, 1500mV/fC). The analog output and a pixel leakage current monitor with equivalent gain ≈8GΩ can be routed to two global analog outputs through digital settings.

One threshold and two window discriminators follow the shaper output. The five threshold levels are coarsely set through external voltages common to all channels. Each threshold level of the two windows can be individually adjusted through a 6-bit DAC with 1.6mV steps. Each discriminator is followed by a 24-bit counter (three counters per channel). During the data readout phase, the counters of all 32 channels are converted into a single shift register for serial readout.

A serial peripheral interface is included for global settings, monitor enabling, channel masking, DACs setting, and counters readout. The channel layout area is 5854µm long times 102µm wide, with 1929µm dedicated to the comparators and DACs and 690µm to the three 24-bit counters.

The power dissipated by the overall chain is 8mW, with 3mW dedicated to the preamplifier.

IV. Front-End Interconnects

Four pixel-to-electronics interconnect solutions were initially considered: (i) adoption of strips in place of pixels to minimize the wire-bond length to the input pads of the front-end ASICs; (ii) metal traces integrated with the Si sensor to bring the wire-bond pads closer to the input pads of the front-end ASICs, (iii) adoption of pixellated ASIC layout with low capacitance ball grid array for direct bump-bonding to the pixellated Si sensor, and (iv) direct wire-bond of each pixel to the input pads of the front-end ASIC.

The major drawback of solution (i) was the increase in perimeter/area ratio when compared to square pixel, with consequent degradation of the spectral quality due to increase in capacitance and charge sharing.

Solution (ii) was limited, along with the excessive interconnect capacitance C_p, by the contribution to the ENC from the dielectric losses associated to C_p (polyimide, SiO_2, Si_3N_4 were considered). This contribution is given by [5]:

$$\delta ENC_{loss} \approx \sqrt{2kT\,C_p\,tan(\delta)} \qquad (1)$$

where δ is the dielectric loss coefficient of the material. For example, in the case of Si_3N_4 (assuming $\varepsilon_r \approx 6.5$, $tan(\delta) \approx 0.001$) with dielectric thickness 3µm, for a 6mm × 10µm interconnect line, a parasitic capacitance $C_p \approx 1.2$pF had to be expected with an unacceptable dielectric contribution $\delta ENC_{loss} \approx 20$ rms electrons (increase in ENC due to C_p an additional issue).

Drawbacks of the solution (iii) were the ball grid material which, if not carefully selected could lead to anomalous fluorescence peaks in the measured spectra, and the constraints imposed on the area and layout of the ASIC (it would also prevent the use of the same ASIC for the Si strip versions), plus the obstacle to illuminating the detector on the pixel side for test purposes.

The solution (iv) was eventually adopted, considering tolerable the complexity of the structure and parasitic capacitance of the bond (≈50-200fF) when compared to pixel and other parasitics (≈920-1220fF). Stability and microphonics related to the length of the bonds, originally considered an issue, have shown to be of negligible effect throughout the first phase of measurements.

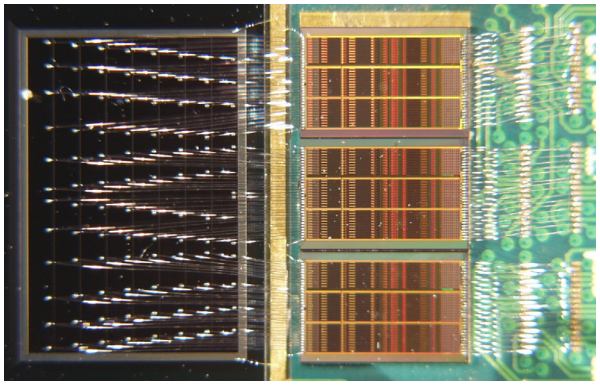

Fig. 4. Photo of a single-quadrant prototype. The 96 pixels are wire-bonded to the inputs pads of three 32-channel ASICs.

Single-quadrant prototypes (96 pixels) were assembled and tested up to now (see Figure 4). Corresponding experimental results are reported in Section VI.

V. Readout Interface

In order to set and read-out the 32-channel ASICs an interface board was developed at NSLS. It includes one Microcontroller module (MC78VZ328), RAM, two DACs, RS232 and Ethernet interfaces. It offers multichannel analyzing capability through the implementation of one high-resolution peak detector, recently developed at the Instrumentation Division [7] and one ADC.

A software with user-friendly interface aimed to fully control the overall system was also developed. It provides several useful functions along with multi-channel analyzer and automatic threshold equalization.

VI. First Experimental Results

Up to now single-quadrant prototypes (96 pixels) were assembled and characterized. Resolution versus temperature, pixel gap, pixel rate, and switching noise from the digital circuitry of the ASIC were investigated.

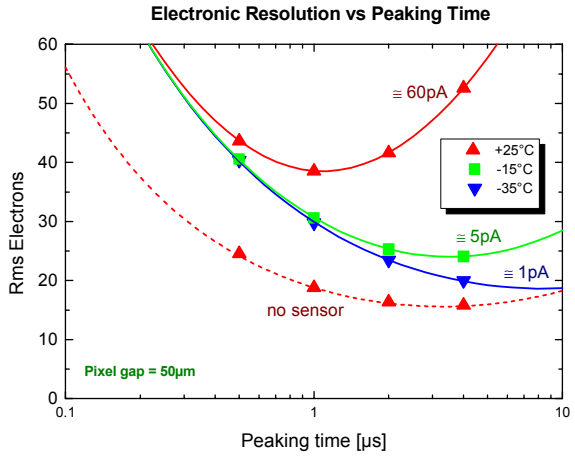

Fig. 5. Measured electronic resolution (ENC) versus peaking time at different temperatures for a pixel with 50µm gap. The ENC without bonding the pixel to the ASIC input pad is also shown.

In Figure 5 the electronic resolution (ENC) as function of the peaking time for a pixel with 50µm gap is shown. The resolution was initially measured at room temperature without bonding the pixel to the ASIC input pad (up triangle, dashed line) and with the pixel bonded (up triangle, solid line). About 14 rms electrons were measured at 4µs peaking time in the first case, to be compared to 39 rms electrons at 1µs in the second case. The corresponding increase in ENC at short peaking times is related to the increase in input capacitance, from 220fF (ASIC bonding pad) to ≈1050fF (wire-bond, pixel). The increase in ENC at long peaking times is related to the pixel leakage current, being about 60pA for this sample. Cooling down at -15°C and -35°C the leakage current decreases and the resolution improves achieving 20 rms electrons at 4µs peaking time.

In Figure 6 the spectrum of a Fe^{55} source measured at –35°C with 4µs peaking time and for a pixel with 50µm gap is shown. A FWHM of 205eV (167eV=20e^- due to electronic noise) at Mn-Kα peak can be extracted. The average resolution for this

kind of pixel was around 220eV, with a +/-7% dispersion and a negligible number of very noisy channels. In Figure 6 the Si escape from Mn-Kα can also be observed.

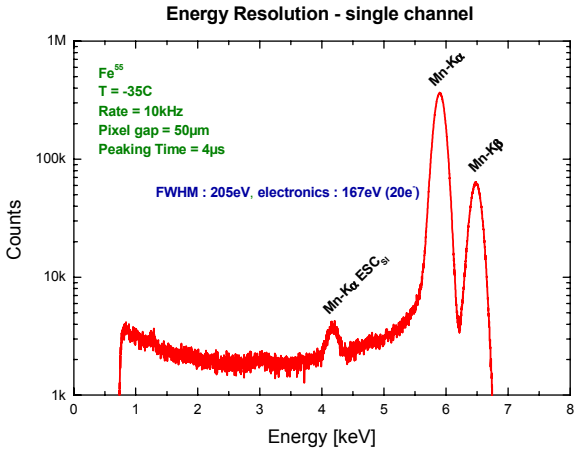

Fig. 6. Spectrum of a ^{55}Fe source measured at -35°C. The FWHM of Mn-Kα peak is 205eV (167eV=20e$^-$ are from electronic noise).

A version of the Si sensor with pixel gaps variable from 6µm to 15µm in steps of 1µm was characterized. In Figure 7 the Fe^{55} spectra, compared to the 50µm gap case, are shown. The better spectral quality (FWHM, peat-valley, and peak-tails) of the 50µm case is due to the lower pixel capacitance (about 700fF plus interconnect, to be compared to about 1000fF plus interconnect for the 10µm case). No appreciable degradation due to fixed charges in oxide for the large gap [3] was observed at this level. The width of the charge sharing region, which occurs along the perimeter of each pixel, was evaluated to be not higher than 25µm in this case.

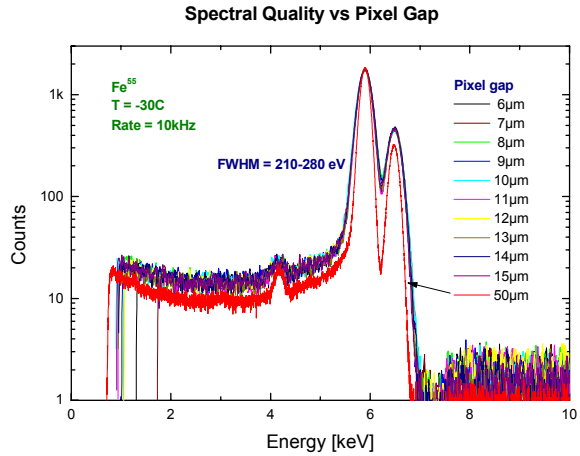

Fig. 7. Spectra of a ^{55}Fe source measured at -30°C for pixel gaps 6-15µm and 50µm.

Layout techniques aimed to minimize the impact of mixed signal activity (from comparators, counters and adjacent channels) on the resolution were adopted. In Figure 8 the effect of switching noise on the resolution for a spectrum of a Fe^{55} source measured at –30°C with 4µs peaking time and for 10µm pixel gap is shown. No degradation was observed starting from a fully analog single channel activity and progressively enabling adjacent channels, discriminators, and counters.

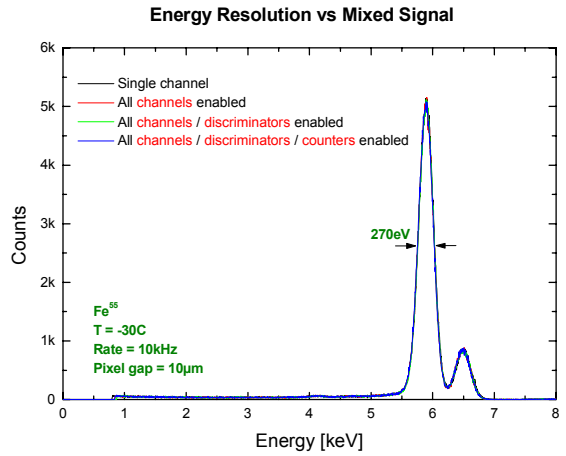

Fig. 8. Spectra of a ^{55}Fe source measured at -30°C for pixel gap 10µm while progressively enabling all channels, discriminators and counters.

In Figure 9 the dependence of the resolution on the rate, expressed in terms of Mn-Kα FWHM of Fe^{55} source for 10µm pixel gap is shown. Two slopes can be observed on the 4µs and 2µs curves, the first attributed to pile-up degradation, the second due to the baseline stabilization circuitry. A resolution at 100kHz of 350eV for 1µs peaking time was measured, to be compared to about 300eV measured on pixels with 50µm gap.

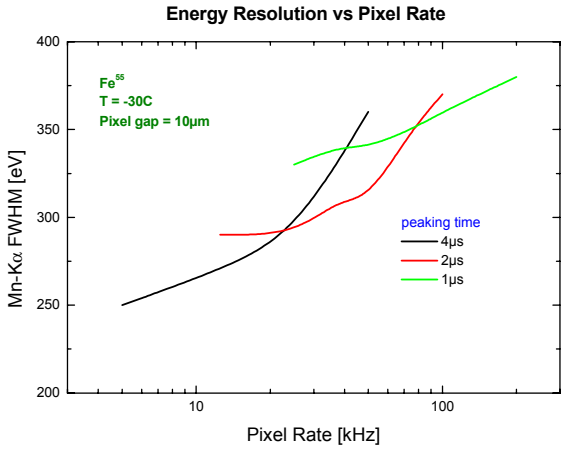

Fig. 9. Resolution expressed in Mn-Kα FWHM of Fe^{55} source measured as function of the pixel rate for different peaking times.

The channel-to-channel threshold dispersion before and after DACs adjustment was also measured and it is shown in Figure 10. The standard deviations, before and after, correspond to 170 and 2.5 rms electrons.

Noise measurements made with threshold scans, direct measurement of the analog monitor output, and X-ray resolution are in good agreement. A baseline shift with temperature less than one mV was also observed.

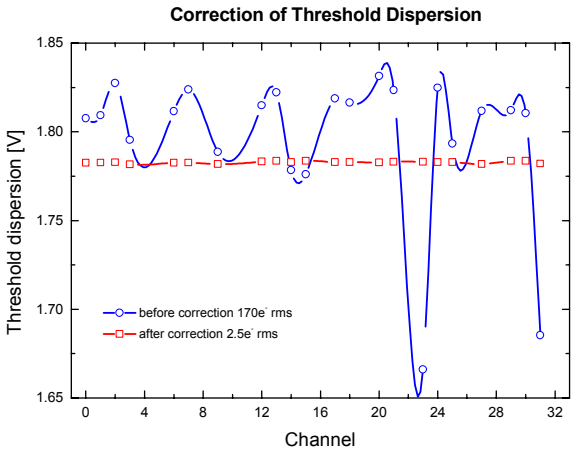

Fig. 10. Measured threshold dispersion before (circles) and after (squares) DACs adjustment.

VII. Conclusions and Future Work

First experimental results on single quadrant (96 pixels) prototypes show stability, rate, resolution and uniformity within expectations. The version with larger pixel gap of 50µm appears preferable in terms of spectral quality. Prototypes with gap larger than 50µm may be considered for next fabrication cycle.

The full four-quadrant version (384 pixels) will be assembled and tested in near future. Overall results indicate that this version should approach the required 40MHz rate with a resolution on the order of 300eV.

For optimization purposes, a second ASIC iteration and a second sensor iteration are being considered.

VIII. Acknowledgment

The authors are very grateful to D. Pinelli and J. Triolo for the excellent technical support. They are in debt with A. Kandasamy, V. Radeka, P.Rehak, G. C. Smith for effective discussions throughout the design, layout and test phases of the project.

IX. References

[1] P. Lechner, C. Fiorini, R. Hartmann, J. Kemmer, N. Krause, P. Leutenegger, A. Longoni, H. Soltau, D. Stötter, R. Stötter, L. Strüder, and U. Weber, "Silicon drift detectors for high count rate X-ray spectroscopy at room temperature", *Nucl. Instr. Meth.*, vol. A458, pp. 281-287, 2001.

[2] A. D. Smith, J. E. Bateman, G. E. Derbyshire, D. M. Duxbury, J. Lipp, E. J. Spill, and R. Stephenson, "A gas microstrip X-ray detector for soft energy fluorescence EXAFS", *Nucl. Instr. Meth.*, vol. A458, pp. 281-287, 2001.

[3] C. Rossington Tull, B. A. Ludewigt, and D. Lewak, "Spectral response of multi-element Silicon x-ray detectors", *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 421-427, 1998.

[4] G. De Geronimo, and P. O'Connor, "A CMOS fully compensated continuous reset system", *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 1458-1462, 2000.

[5] G. De Geronimo, P. O'Connor, and Joe Grosholz, "A generation of CMOS readout ASICs for CZT detectors", *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 1857-1867, 2000.

[6] G. De Geronimo, and P. O'Connor, "A CMOS baseline holder for readout ASICs", *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 818-822, 2000.

[7] G. De Geronimo, P. O'Connor, and A. Kandasamy, "Analog CMOS peak detect and hold circuit – Part 2. The two-phase offset free and derandomizing configuration", *Nucl. Instr. Meth.*, vol. A484, pp. 544-556, 2002.